WE CLAIM:

1. A chemical vapor deposition (CVD) method for forming a compound comprising Ta and N, comprising the steps of:

using an alkylimidotris(dialkylamido)Ta species for Ta precursor; and

providing a precursor supplying nitrogen.

2. The method of claim 1, further comprising the step of selecting tertiaryamylimidotris(dimethylamido)Ta as said alkylimidotris(dialkylamido)Ta species.

3. The method of claim 1, further comprising the step of selecting ammonia for said precursor supplying nitrogen.

4. The method of claim 1, further comprising the step of selecting said compound from the group consisting of TaN and TaSiN.

5. The method of claim 4, further comprising the step of selecting the N to Ta elemental ratio in said compound to be greater than about 0.9.

6. The method of claim 4, further comprising the step of selecting a Si precursor for said TaSiN from the group consisting of silane and disilane.

7. The method of claim 1, further comprising the step of using hydrogen for carrier gas.

8. A semiconductor field effect device having a gate dielectric and a gate, wherein said gate comprises a compound comprising Ta and N disposed over said gate dielectric, wherein said compound has a resistivity below about 20mΩcm, and wherein in said compound the elemental ratio of N to Ta is greater than about 0.9.

9. The field effect device of claim 8, wherein said compound is TaN or TaSiN.

10. The field effect device of claim 9, wherein in said TaN the N to Ta elemental ratio is between about 0.9 and 1.1.

11. The field effect device of claim 10, wherein said TaN has a crystalline material structure.

12. The field effect device of claim 9, wherein in said TaSiN the Si to Ta elemental ratio is between about 0.35 and 0.5.

13. The field effect device of claim 12, wherein said TaSiN has an substantially amorphous material structure.

14. The field effect device of claim 9, wherein said TaSiN has a workfunction which equals an n-doped Si workfunction within about 300mV.

15. The field effect device of claim 8, wherein said gate dielectric has an equivalent oxide thickness of less than about 5nm.

16. The field effect device of claim 15, wherein said gate dielectric has an equivalent oxide thickness of less than about 2nm.

17. The field effect device of claim 8, wherein said gate dielectric comprises SiO_2.

18. The field effect device of claim 8, wherein said gate dielectric comprises a high-k dielectric material.

19. The field effect device of claim 8, wherein said device is a Si based MOS transistor.

20. The field effect device of claim 19, wherein said device is an NMOS transistor.

21. The field effect device of claim 20, wherein said NMOS transistor has a threshold voltage between about 0.15V and 0.55V.

22. A method for fabricating a semiconductor field effect device which has a gate dielectric, comprising the step of depositing onto said gate dielectric a compound comprising Ta and N by using chemical vapor deposition (CVD) with an alkylimidotris(dialkylamido)Ta species for Ta precursor.

23. The method of claim 22, further comprising the step of selecting said compound with a resistivity below about 20mΩcm.

24. The method of claim 22, further comprising the step of selecting in said compound the elemental ratio of N to Ta to be greater than about 0.9.

25. The method of claim 22, further comprising the step of selecting said compound from the group consisting of TaN and TaSiN.

26. The method of claim 25, further comprising the step of selecting the N to Ta elemental ratio in said TaN to be between about 0.9 and 1.1.

27. The method of claim 25, further comprising the step of selecting the Si to Ta elemental ratio in said TaSiN to be between about 0.35 and 0.5.

28. The method of claim 22, further comprising the step of selecting tertiaryamylimidotris(dimethylamido)Ta as said alkylimidotris(dialkylamido)Ta species.

29. The method of claim 22, further comprising the step of heating said compound up to about 1000°C.

30. The method of claim 22, further comprising the step of providing a source and a drain, wherein the step of depositing said compound is carried out before the step of providing said source and said drain.

31. The method of claim 22, further comprising the step of providing a source and a drain, wherein the step of depositing said compound is carried out after the step of providing said source and said drain.

32. The method of claim 22, wherein said step of depositing is carried out conformally onto a patterned surface.

33. A processor, comprising:

at least one chip, wherein said chip comprises at least one semiconductor field effect device having a gate dielectric and a gate, wherein said gate comprises a compound comprising Ta and N disposed over said gate dielectric, wherein said compound has a

resistivity below about 20mΩcm, and wherein in said compound the elemental ratio of N to Ta is greater than about 0.9.

34. The processor of claim 33, wherein said processor is a digital processor.

35. The processor of claim 33, wherein said processor comprises at least one analog circuit.